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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,598	07/23/2003	Masayoshi Tojima	60188-616	7624

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EXAMINER	
SORRELL, ERON J	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,598	TOJIMA ET AL.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9,11 and 12 is/are rejected.

7)☒ Claim(s) 10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/23/03; 10/17/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Margulis (U.S. Pub. No. 2001/0040580).

3. Referring to claim 1, Margulis teaches a semiconductor integrated circuit device (see figure 5) that operates while being connected to an external processing unit (see connection to CPU subsystem), comprising:

a plurality of internal memories (see items 5 in figure 5);

a first processing unit for data processing (see item 506 in figure 5) and a second processing unit for data processing (see item 508 in figure 5); and

a memory configuration controller (item 512 in figure 5) for controlling the assignment of the plurality of internal memories to the first processing unit, the second processing

unit and the external processing unit in accordance with an application (see paragraph 32 on page 2).

4. Referring to claim 3, Margulis teaches the memory configuration controller further has the function to control the assignment of an external memory to the first processing unit, the second processing unit and the external processing unit, in accordance with an application (see paragraph 32 on page 2).

5. Referring to claim 4, Margulis teaches the memory configuration controller comprises a first register (see item 804 in figure 8) for specifying the assignment of the plurality of internal memories and the external memory (see paragraph 45 on page 4); and

wherein data transfer between the first to third data buses is accomplished by rewriting the content of the first register (see paragraph 45 on page 4).

6. Referring to claim 5, Margulis teaches the first register is configured such that it can specify which of the plurality of internal memories and the external memory is unused (see paragraph 45, note this information can be derived from the status information).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2,7-10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Margulis in view of Kosugi et al. (U.S. Patent No. 6,640,019 hereinafter "Kosugi").

9. Referring to claim 2, Margulis teaches the semiconductor integrated circuit device further comprises:

a first data bus (see item 534 in figure 5) connected to the first processing unit (see item 506 in figure 5);

a second data bus (see item 536 in figure 5) connected to the second processing unit (see item 508 in figure 5);

third data bus dedicated to the external processing unit(see bus connecting CPU subsystem to CPU, not shown);

a first memory interface, which is interposed between the memory assigned to the first processing unit and the first data

bus (see items IMC 1-N and EMC 1-N, these items are the interfaces to the internal and external memories, respectively);

a second memory interface, which is interposed between the memory assigned to the second processing unit and the second data bus (see items IMC 1-N and EMC 1-N, these items are the interfaces to the internal and external memories, respectively); and

a third memory interface, controlling a data transfer, which is interposed between the memory assigned to the external processing unit and the third data bus (see items IMC 1-N and EMC 1-N, these items are the interfaces to the internal and external memories, respectively).

Margulis fails to teach the first and second memory interfaces handling a DMA data transfer.

Kosugi teaches in an analogous system, at least first and second memory interfaces that handle DMA transfers between memories (see DMAC 107,112, and 115 in figure 3 and lines 64 of column 3 to line 30 to column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Margulis with the above teachings of Kosugi, such that the memory interfaces handle DMA transfers. One of ordinary skill in the art would have been motivated to make this

modification in order to relieve the host processor the burden of processing numerous data transfers.

10. Referring to claim 7, Margulis teaches the semiconductor integrated circuit further comprises:

a first bus selector for selectively connecting the first processing unit with the first or the second data bus (see MUX in figures 9 and 10 and paragraph 54); and

a second bus selector for selectively connecting the second processing unit with the first or the second data bus (see MUX in figures 9 and 10 and paragraph 54, note a this large MUX can be implemented as a plurality of smaller MUX's).

11. Referring to claim 8, Margulis teaches the first processing unit comprises a local memory and data is transferred to/from the local memory to/from the memory assigned to the first processing device (see paragraph 74 on page 6).

Margulis fails to teach DMA data transport carried out between the memories.

Kosugi teaches in an analogous system, at least first and second memory interfaces that handle DMA transfers between memories (see DMAC 107,112, and 115 in figure 3 and lines 64 of column 3 to line 30 to column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Margulis with the above teachings of Kosugi, such that the memory interfaces handle DMA transfers for the same reasons as mention in the rejection of claim 2, supra.

12. Referring to claim 9, Margulis teaches the semiconductor integrated circuit device further comprises:

a host interface that is interposed between the external processing unit and the third data bus (see item 504 in figure 5); and

a third bus selector for selectively connecting the host interface with the first or the second data bus (see MUX in figures 9 and 10 and paragraph 54, note a this large MUX can be implemented as a plurality of smaller MUX's).

13. Referring to claim 10, Margulis teaches the semiconductor integrated circuit device further comprises a fourth bus selector for selectively connecting the third data bus with the third memory interface or the second data bus (see MUX in figures 9 and 10 and paragraph 54, note a this large MUX can be implemented as a plurality of smaller MUX's).

14. Referring to claim 12, Margulis fails to explicitly teach the claimed integrated circuit is a portable device, however, Kosugi teaches, the above limitation (see lines 49-53 of column 14).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's to use the IC in a portable device, because these devices are generally small and would benefit from shared memory usage for graphics processing as suggested by Margulis (note this rejection is applicable to all claims rejected in view of Margulis and/or Kosugi).

15. Claim 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Margulis in view of Fukuda et al. (U.S. Patent No. 5,619,676 hereinafter "Fukuda").

16. Referring to claim 6, Margulis fails to teach the memory configuration controller comprises a second register for specifying the respective storage capacities of the plurality of internal memories and the external memory.

Fukuda teaches, in an analogous system, a register for specifying the respective storage capacities of the plurality of memories (see lines 50-59 of column 8).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Margulis with the above teachings of Fukuda. One of ordinary skill in the art would have been motivated to make such modification in order to provide for optimal memory usage for the separate processing modules.

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Margulis in view of Fukuda et al. (U.S. Patent No. 5,619,676 hereinafter "Fukuda") and further in view of Kosugi.

18. Referring to claim 12, the combination of Margulis and Fukuda fails to explicitly teach the claimed integrated circuit is a portable device, however, Kosugi teaches, the above limitation (see lines 49-53 of column 14).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's to use the IC in a portable device, because these devices are generally small and would benefit from shared memory usage for graphics processing as suggested by Margulis.

Allowable Subject Matter

19. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or suggest alone or in combination supplying a relative address from an external processing unit when a fourth bus selector selects a connection between a third data bus and the third memory interface and an absolute address is provided from an external processing unit when the fourth bus selector selects a connection between the third data bus and a second data bus, ***in combination with the other claimed limitations*** (emphasis added).

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited to further show the state of the art as it pertains to the applicant's invention:

U.S. Patent No. 4,827,406 to Bischoff et al. teaches a method and system for allocating memory between multiple processors; and

U.S. Patent No. 6,195,733 to Nair et al. teaches sharing memory between multiple processors in a single chip multiprocessor system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

KIM HUYNH
SUPERVISORY PATENT EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
March 14, 2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER

3/19/06